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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 09/588,072 | 06/05/2000 | Ahmed Saifuddin | QCPA000320 | 8110 |

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| EXAMINER | |
|---|---|
| TORRES, JOSEPH D | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2133 | 4 |

DATE MAILED: 03/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/588,072 | SAIFUDDIN ET AL. | |
| | Examiner | Art Unit | |
| | Joseph D. Torres | 2133 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *12 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *9-34* is/are pending in the application.

4a) Of the above claim(s) *16-34* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 January 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Election/Restrictions*

1. Applicant's election without traverse of Group I, claims 9-15, in Paper No. 19 is acknowledged.

Claims 16-34 withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to nonelected inventions, there being no allowable generic or linking claim. Election was made **without** traverse in Paper No. 19.

### *Response to Arguments*

2. Applicant's arguments with respect to claims 9-15 have been considered but are moot in view of the new ground(s) of rejection.

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.

2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claims 9-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nagasawa; Kenichi et al. (US 5446744 A, hereafter referred to as Nagasawa) in view of Wright, David A. (US 6445702 B1).

35 U.S.C. 103(a) rejection of claim 9.

Nagasawa teaches a method comprising: receiving a plurality of information bits, the plurality of information bits containing different classes of information bits (Figure 6 in Nagasawa teaches 5 classes of information bits comprising a plurality of information bits: Sync. Code information bits, Transmission Id information bits, A Check Bit information bit, Boundary Information bits and Image Information bits); determining an outer quality metric in accordance with the plurality of information bits (Figure 6 in Nagasawa teaches that C2 parity is applied to the plurality of information bits; col. 7, lines 43-48 in Nagasawa teaches that C2 parity is an outer code; col. 7, lines 39-41 in Nagasawa teaches that the C2 parity is a Reed-Solomon code; Note: a Reed-Solomon code is an error detection and correction code capable of detecting the number of correctable and uncorrectable errors and is capable of providing an explicit measure of data integrity and/or quality, hence the C2 parity is an outer quality metric) and an inner quality metric in accordance with at least one group of information bits of a particular class (Figure 6 in Nagasawa teaches that C1 parity is applied in accordance with at least one group of information bits of a particular class; col. 7, lines 49-53 in Nagasawa

teaches that C1 parity is an inner code; col. 7, lines 39-41 in Nagasawa teaches that the C1 parity is a Reed-Solomon code; Note: a Reed-Solomon code is an error detection and correction code capable of detecting the number of correctable and uncorrectable error and is capable of providing an explicit measure of data integrity and/or quality, hence the C1 parity is an inner quality metric); and forming an ECC block comprising the plurality of information bits, the outer quality metric, and the inner quality metric, the outer quality metric being used for protection of the plurality of information bits and the inner quality metric being used for protection of the at least one group of information bits of the particular class (the ECC block of Figure 6 of Nagasawa is a transmission format comprising the plurality of information bits, the outer quality metric, and the inner quality metric, the outer quality metric being used for protection of the plurality of information bits and the inner quality metric being used for protection of the at least one group of information bits of the particular class).

However Nagasawa, does not explicitly teach that the ECC block of data in Figure 6 of Nagasawa is a frame, that is, that the entire error correction block or error correction unit is also a frame.

Wright, in an analogous art, teaches a block error correction unit, which includes inner and outer parity codes whereby the entire error correction block or error correction unit is also a frame. The Examiner would like to point out that Wright teaches that the error correction block is formed into a frame to avoid complex processing at the transmission side (col. 1, lines 25-45), hence one of ordinary skill in the art at the time the invention was made would be highly motivated to combine the patents since Wright teaches that

the error correction block is formed into a frame and Nagasawa teaches the specifics of a block error correction code with both an inner and outer code required by the Wright patent.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Nagasawa with the teachings of Wright by employing error correction blocks or error correction units that are also frame units. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that employing error correction blocks or error correction units that are also frame units would have provided the opportunity to avoid complex processing at the transmission side (col. 1, lines 25-45).

35 U.S.C. 103(a) rejection of claim 10.

Col. 7, lines 39-41 in Nagasawa teaches that the C2 parity is a Reed-Solomon code and since a Reed-Solomon code is a cyclic redundancy code, the C2 outer quality metric is a CRC code.

35 U.S.C. 103(a) rejection of claim 11.

Figure 6 in Nagasawa teaches that the C2 outer quality metric includes at least 1 parity bit; hence the C2 outer quality metric comprises a parity bit.

35 U.S.C. 103(a) rejection of claim 12.

Col. 7, lines 39-41 in Nagasawa teaches that the C1 parity is a Reed-Solomon code and since a Reed-Solomon code is a cyclic redundancy code, the C1 inner quality metric is a CRC code.

35 U.S.C. 103(a) rejection of claim 13.

Figure 6 in Nagasawa teaches that the C1 inner quality metric includes at least 1 parity bit; hence the C1 inner quality metric comprises a parity bit.

35 U.S.C. 103(a) rejection of claim 14.

Nagasawa teaches transmitting the frame to a destination (See Figure 1 in Nagasawa); receiving the frame at the destination (see Memory 106 in Figure 1 of Nagasawa); and determining whether the frame has been correctly received based on the outer quality metric contained in the frame (Error Correction Unit 107 determines whether the frame has been correctly received based on the outer quality metric contained in the frame).

4. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nagasawa; Kenichi et al. (US 5446744 A, hereafter referred to as Nagasawa) and Wright, David A. (US 6445702 B1) in view of Tanaka; Mitsugu (US 5740187 A).

35 U.S.C. 103(a) rejection of claim 15.

Nagasawa and Wright, substantially teach the claimed invention described in claims 9-14 (as rejected above).

However Nagasawa and Wright do not explicitly teach the specific use of a decoder for decoding the ECC block taught in the Nagasawa patent.

Tanaka, in an analogous art, teaches the decoder required for decoding the ECC blocks taught in the Nagasawa patent. Tanaka teaches that if the frame has not been received correctly, determining whether the at least one group of information bits has been received correctly based on the inner quality metric contained in the frame; and recovering the at least one group of information bits if the inner quality metric indicates that the at least one group of information bits has been received correctly (Inner Code Decoding Block in Figure 1 of Tanaka teaches a means for determining whether the at least one group of information bits has been received correctly based on the inner quality metric contained in the frame and recovering the at least one group of information bits if the inner quality metric indicates that the at least one group of information bits has been received correctly prior to sending the data to the Outer Code Decoding Block in Figure 1 of Tanaka). The Examiner asserts that one of ordinary skill in the art at the time the invention was made would have been highly motivated to combine the Tanaka patent with the teachings in the Nagasawa and Wright patents since the decoder in the Tanaka patent is the required decoder for decoding the ECC blocks taught in the Nagasawa patent.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Nagasawa and Wright with the teachings of Tanaka by including use of a decoder for decoding the ECC block taught in the Nagasawa patent. This modification would have been obvious to one of ordinary skill in the art, at the time

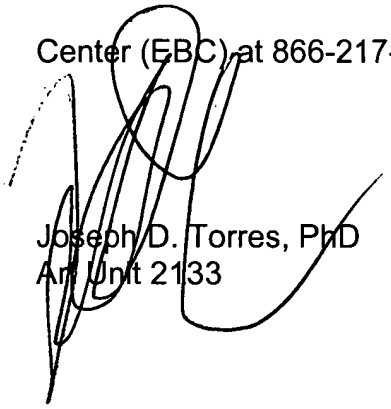
the invention was made, because one of ordinary skill in the art would have recognized that use of the decoder in the Tanaka patent for decoding the ECC block taught in the Nagasawa patent would have provided the opportunity to decode the ECC blocks in the Nagasawa patent since the decoder in the Tanaka patent is the required decoder for decoding the ECC blocks taught in the Nagasawa patent.

***Conclusion***

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (703) 308-7066. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Joseph D. Torres, PhD
Art Unit 2133